A NOVEL CPW STRUCTURE FOR HIGH-SPEED INTERCONNECTS

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Abstract—**For high-speed digital circuits a novel elevated-CPW (ECPW) structure with low loss and low dispersion is proposed and the performances are well compared with the theoretical prediction. The ECPW is designed with the aid of time domain fullwave FDTD technique and is fabricated using conventional thick-film MEMS processing. Proposed structure reveal at least 10dB lower insertion loss compared to conventional CPW geometries and effective permittivity is 4 to 6 times smaller than that of conventional CPW. Characteristic impedances and effective permittivities are given for various geometrical parameters.**

I. INTRODUCTION

Coplanar waveguide (CPW) is a fundamental and important element for MMICs due to its ease of mounting active devices. Unfortunately, as frequency increases CPW suffers from dispersion loss caused by air-dielectric material discontinuity which is inherent to substrate-supported transmission lines.

In view of the above, a few CPW transmission line geometries with a low loss and low dispersion in high frequency have been reported. Removal of substrate material under signal line [1,2,3], placing CPW on membrane made by bulk micromachining [4,5], elevating signal line in air using surface micromachining [6] were introduced. These types of CPWs are, however, not economical for mass production and applications are limited. In addition, the mechanical durability of these structures are also questionable. Lately, a new low loss CPW which is mechanically rigid is introduced [7]. However, to use a novel CPW in real applications, further specific investigations of dispersion, characteristic impedance and loss are needed.

In this paper, as a novel CPW, an elevated CPW (ECPW) is introduced. ECPW is the transmission line of which signal line is elevated in the air by using micromachining technique. For the design purposes, characteristic impedances and effective permittivities are given for various geometrical parameters.

II. DESIGN AND FABRICATION

Fig. 1 is the 3-dimensional view of ECPW. The underlying idea of ECPW is based on the fact that by reducing the effect of the air-dielectric material discontinuity and by elevating the signal line in the air the dispersion could be minimized. Also to interconnect the ECPW with other devices, a novel transition structure must be fabricated on the same wafer. Silicon and GaAs are usually used as substrate materials in MMIC, but not limited.

The main fabrication process is as follows. First, for seed-layer of transmission line metal, Cr and Cu is e-beam coated and then copper is plated after PR(Photo Resistor) is coated with photo-lithography. Second, for bridges to support elevated structure, PR is coated as a sacrificial layer and copper is plated. In this second step, the elevation height is determined by controlling the height of the bridges. Third, seed-layer is coated and copper is plated for the signal line of elevated CPW. Fig. 2 is the side view of our fabricated ECPW. Detailed fabrication process is depicted in Fig. 3.

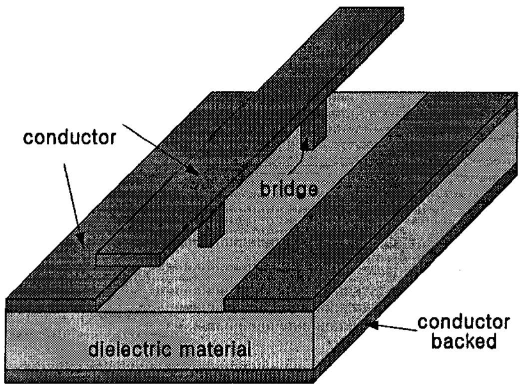

Fig. 1. Newly fabricated elevated CPW

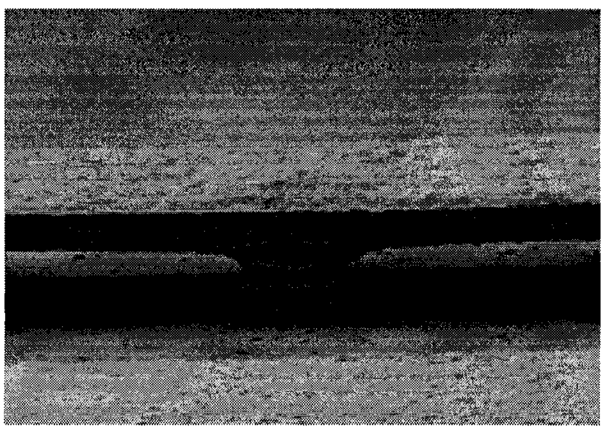

Fig. 2. SEM photo of a fabricated ECPW

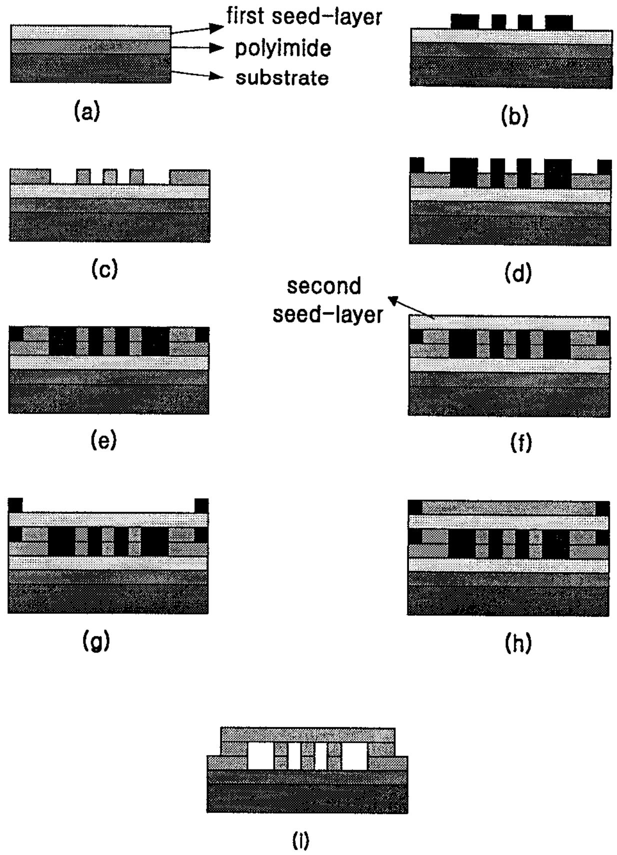

Fig. 3. Fabrication process

(a) polyimide and first seed-layer coating
(b) PR coating and photo-lithography
(c) copper plating
(d) PR coating and photo-lithography
(e) copper plating
(f) second seed-layer coating
(g) PR coating and photo-lithography
(h) copper plating
(i) first and second seed-layer etching

III. RESULT AND ANALYSIS

For the accurate analysis of ECPW geometries, Yee's scheme FDTD technique is developed and applied in this work. For a specific investigation, electrical characteristics are calculated by varying critical geometrical parameters as shown in Fig. 4. In practice, the effect of *d* could be negligible, when *d* exceeds 100 μm, thus substrate thickness is set to 100 μm in calculation. It is found that the most critical geometrical parameters are *h* and *s*.

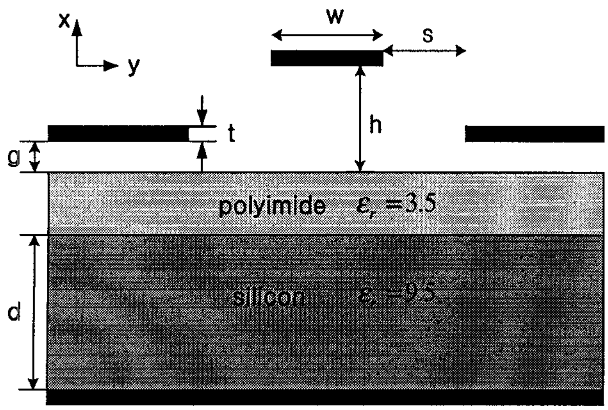

Fig. 4. Cross-section of ECPW(*d*=500 μm, *w*=100 μm, 10 μm polyimide layer thickness, 5 mm line length in z-direction)

A. Characteristic Impedance

Characteristic impedances are calculated by varying *s/w* and *w/h* and results are shown in Fig. 5. It is found that as *h* and *s* increase, the characteristic impedances increase, and this result can be explained from the expression of characteristic impedance in lossless and TEM case[8]:

$$Zo = \sqrt{\frac{L}{C}} \qquad (1)$$

where, *C* and *L* is capacitance and inductance, respectively. Increase of *h* and *s* causes the decrease of capacitance, thus leading to the increase of characteristic impedances. Especially when *s* is negative, which is overlapped configuration, low characteristic impedance can be obtained without enlarging signal line width.

B. Effective Permittivity

Effective permittivity is an important parameter which accounts for the dispersive characteristics[9]. Effective permittivities are also calculated by varying *s/w* and *w/h*, and results are displayed in Fig. 6. It is investigated that the effective permittivity decreases as *h* increases, and this is because the effect of air-dielectric discontinuity is diminished as elevating signal line from substrate. The effective permittivity decreases also when *s* becomes smaller, and this is due to the same reason above.

C. Return loss

The return loss of ECPW is calculated and measured as shown in Fig. 7 and Fig. 8, and it is found that loss decreases as *s* is decreases. Thus, by reducing the effect of air-dielectric material discontinuity the dispersion loss could be significantly reduced.

IV. CONCLUSIONS

It is found that ECPW proposed in this paper has a superior performance for the application to high-speed digital interconnects in that it has 15 to 17 dB lower loss and 4 to 6 times lower effective permittivity than conventional CPW. Various characteristic impedances from 20 Ω to 110 Ω can be obtained easily. Especially, for overlapped structure, very low loss and low effective permittivity can be achieved and in this structure low characteristic impedance are implemented without enlarging the overall circuit size.

ACKNOWLEDGEMENT

This work is partially supported by Yonsei University Research Grant Program and the University Research Program by Ministry of Information and Communication in South Korea

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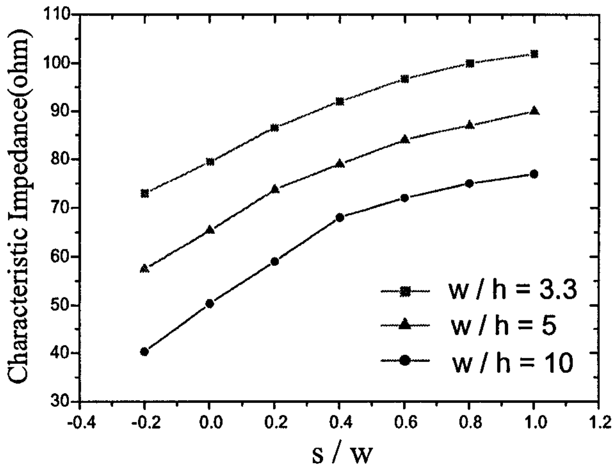

Fig. 5. Characteristic impedances as a function of gap between the center and ground plane, *s*, for different *h*

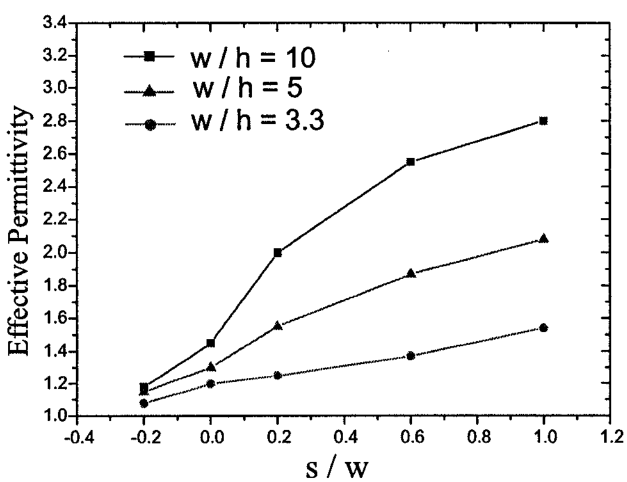

Fig. 6. Effective permittivity as a function of gap between the center and ground plane,*s*,for different *h*

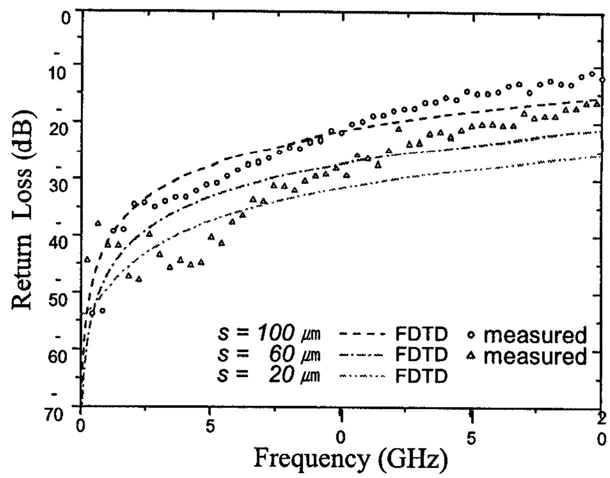

Fig. 7. Return Loss when *h*=0 μm

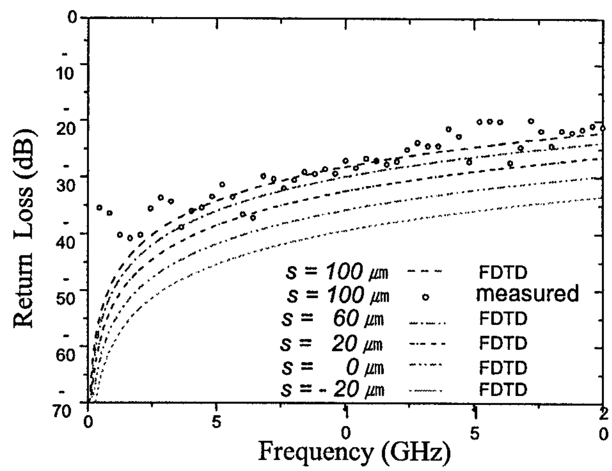

Fig. 8. Return Loss when *h*=10 μm